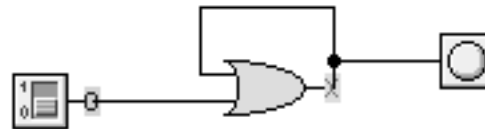


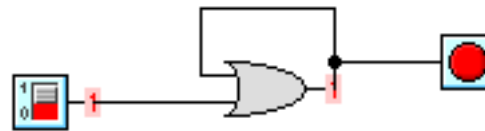
Set Latch

- Before input:



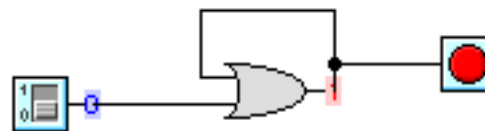
The state of the latch is undefined.

- Input (set) line high:



The state of the latch is logical 1.

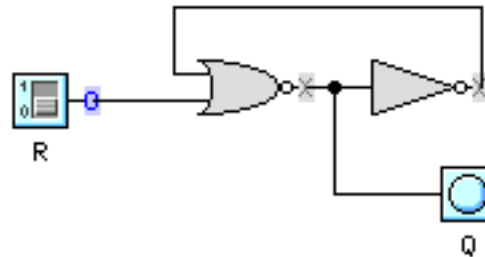
- Input (set) line low:



The state of the latch is permanently set to logical 1. No further inputs will change the state.

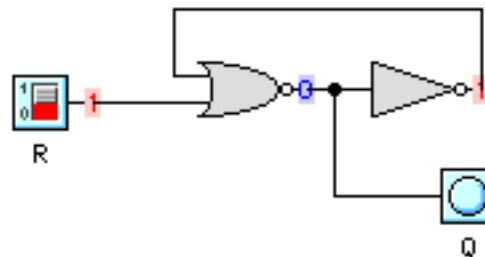
Reset Latch (1)

- Before input:



The state of the latch is undefined.

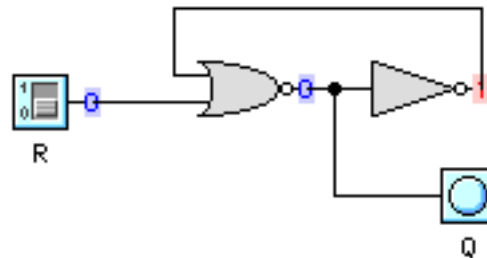
- Input (reset) line high:



The state of the latch is logical 0.

Reset Latch (2)

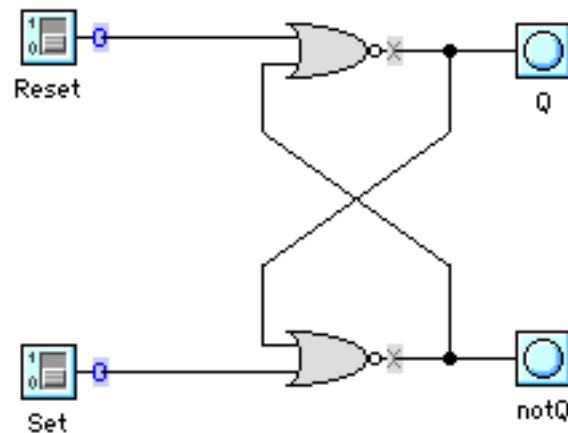
- Input (reset) line low:



The state of the latch is permanently set to logical 0. No further inputs will change the state.

Set-Reset Latch (1)

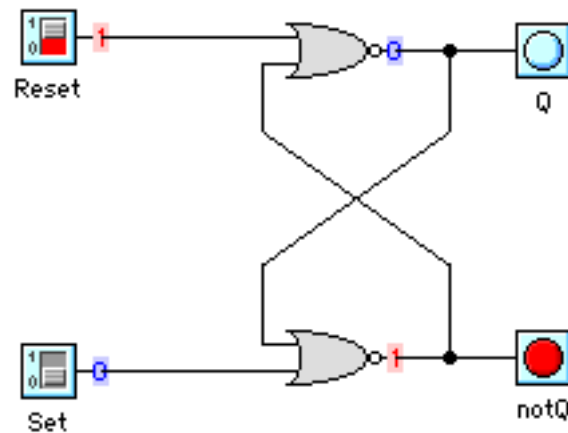
- Before input:



The state of the latch is undefined.

Set-Reset Latch (2)

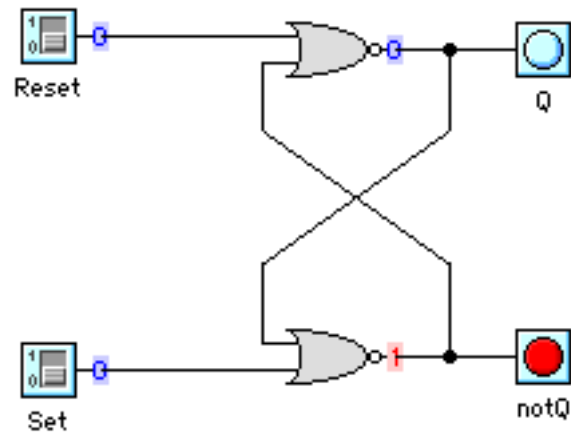
- Reset line high:



The next state (Q^*) of the latch is logical 0.

Set-Reset Latch (3)

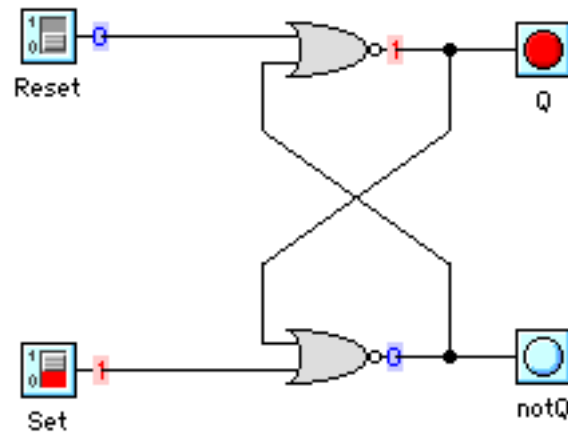
- Reset line returned to low:



The next state (Q^*) of the latch is still logical 0.

Set-Reset Latch (4)

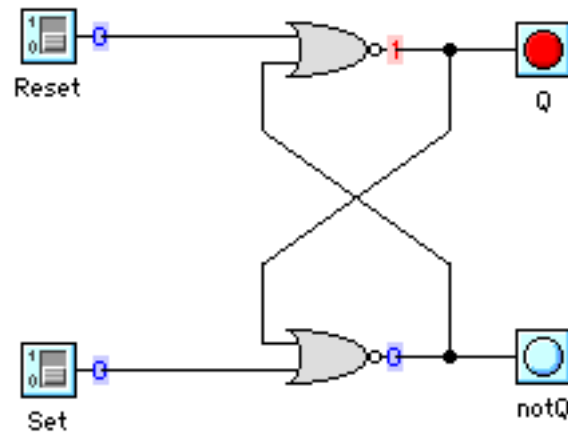
- Set line high:



The next state (Q^*) of the latch is logical 1.

Set-Reset Latch (5)

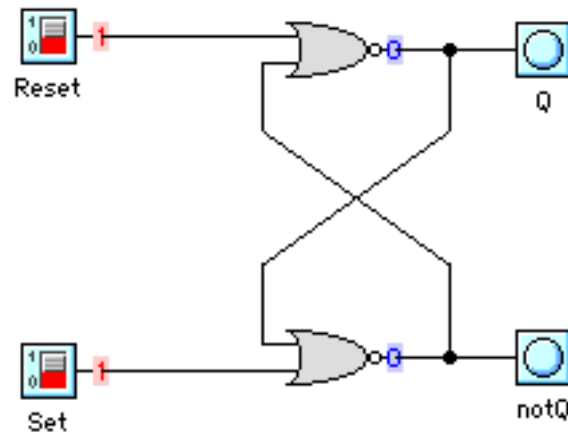
- Set line returned to low:



The next state (Q^*) of the latch is still logical 1.

Set-Reset Latch (6)

- Set and reset lines high:

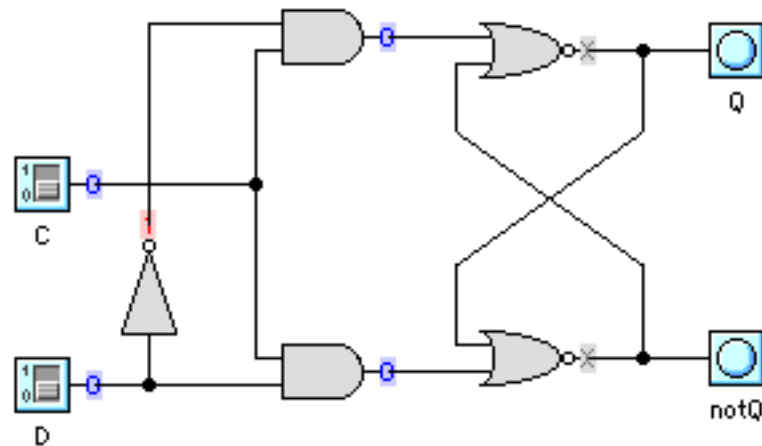


This is an illegal condition called a race condition.

- A race condition is a situation where two gates race each other for control of the state. In a race condition, the next state is undefined.

D Latch (1)

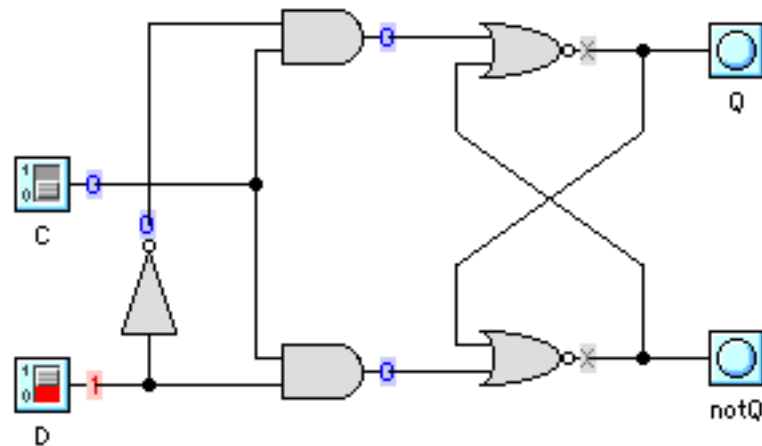
- Before input:



The state of the latch is undefined.

D Latch (2)

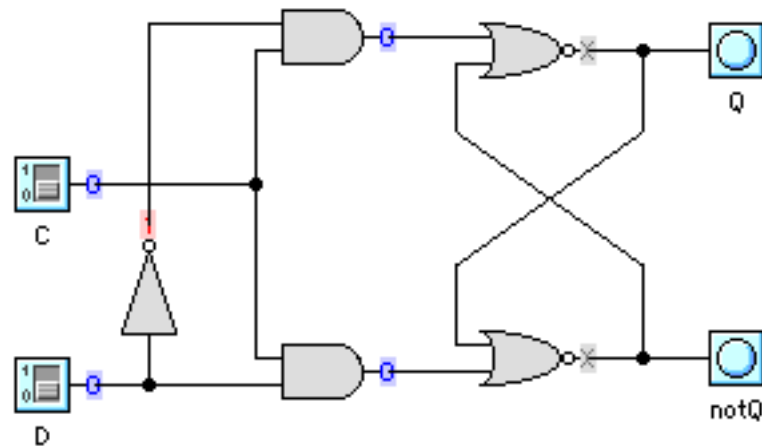
- D input high:



The state of the latch is still undefined, since the clock is not enabled.

D Latch (3)

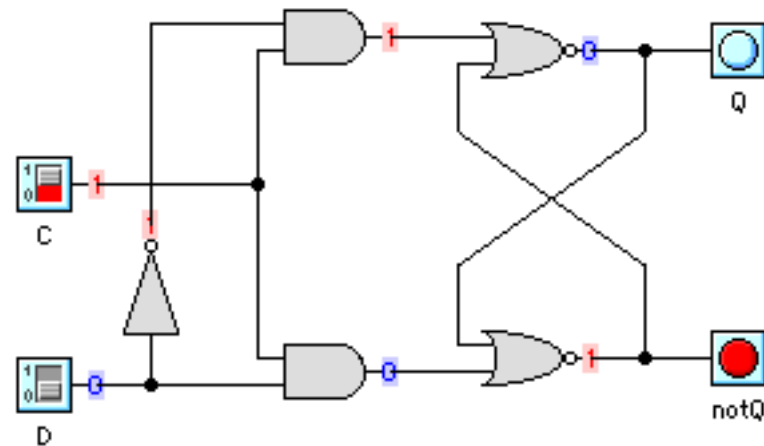
- D input returned to low:



The state of the latch is still undefined.

D Latch (4)

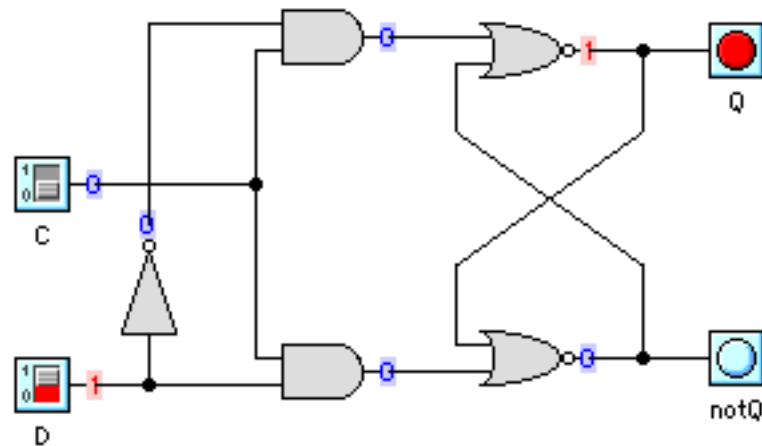
- C input high:



The state of the latch is logical 0, since the input D is logical 0. The state is given by the input D when the clock is enabled.

D Latch (6)

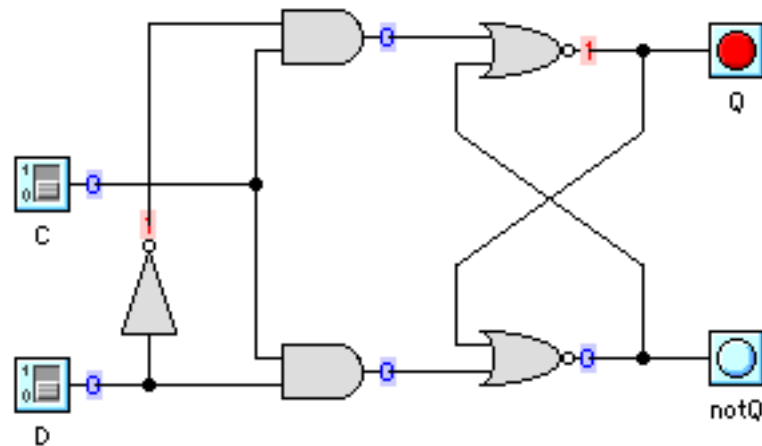
- C input returned to low:



The state of the latch is logical 1.

D Latch (7)

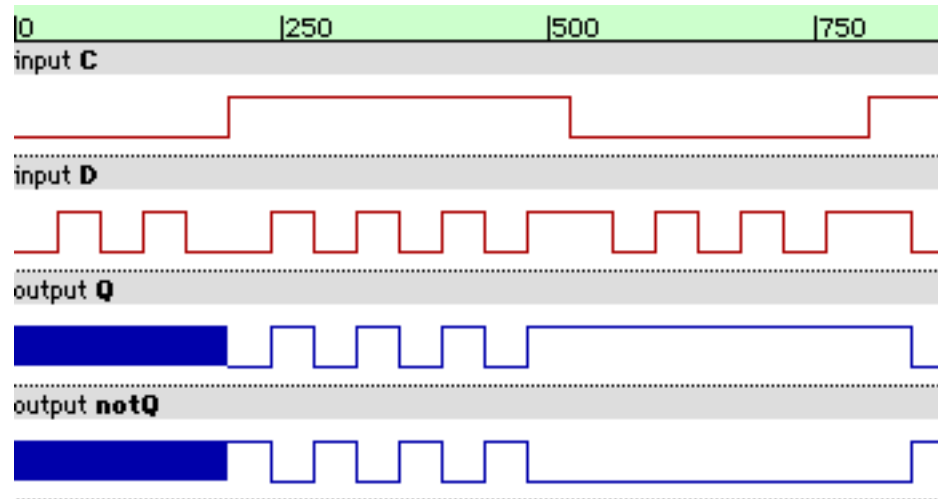
- D input returned to low:



The state of the latch is still logical 1.

D Latch (8)

- Signals:



The state of the latch only allowed to change when the clock signal is enabled and then the input D is passed through to the output.